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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,091	ARAYA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/1/01, 5/23/03*, 9 | 23 | 03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 of the application have been examined.

Foreign Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application P2000-166630 filed in Japan on June 2, 2000. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. Acknowledgment is made of the information disclosure statements filed on June 1, 2001, May 23, 2003 and September 12, 2003 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

4. The drawings submitted on June1, 2001 are accepted.

Specification

5. The disclosure is objected to because of the following informalities:

Page 2, Lines 2-3 state, "simulation platforms (or algorithms) are normally structured without consideration of distinctions between the hardware and software". Specification Page 9, Line 22 states, "Fig. 3 shows an example of the restructured simulation platform". Fig. 3 shows a program listing and does not include the hardware required to perform the simulation such as the computer, the memory, the IO devices etc. as will be understood by one of ordinary skill in the art. Similarly, specification, Page 17, Line 1 states, "In the simulation platform shown in Fig. 10, there are three buses". Again, Fig. 10 shows a program listing and does not include any hardware required for simulation. Therefore, it is assumed that what the applicants meant by "simulation platform" is actually a "simulation program" written in a general purpose language. In order to avoid confusion, the Examiner directs the applicants to change all references to "simulation platform" to "simulation program" in the specification and abstract.

Page 2, Lines 24-25, "it becomes necessary to provide considerably large numbers of codes for use in description of the circuit to be created" appears to be incorrect and it appears that it should be "it becomes necessary to provide considerably large amount of code for use in description of the circuit to be created".

Page 11, Lines 19-20, "evaluation method of the second embodiment that has tree variables a, b and c" appears to be incorrect and it appears that it should be "evaluation method of the second embodiment that has three variables a, b and c".

Appropriate correction is required.

Claim Objections

6. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

7. Claims 1-10 are objected to because of the following informalities:

Claim 1, Lines 8-9 state, "in response to modified sources, structuring a simulation platform for use in an architecture design". Specification Page 9, Line 22 states, "Fig. 3 shows an example of the restructured simulation platform". Fig. 3 shows a program listing and does not include the hardware required to perform the simulation such as the computer, the memory, the IO devices etc. as will be understood by one of ordinary skill in the art. Similarly, specification, Page 17, Line 1 states, "In the simulation platform shown in Fig. 10, there are three buses". Again, Fig. 10 shows a program listing and does not include any hardware required for simulation. Therefore, it is assumed that what the applicants meant by "simulation platform" is actually a "simulation program" written in a general purpose language. In order to avoid confusion, the Examiner directs the applicants to change all references to "simulation platform" to "simulation program" in all claims.

Claim 2 refers to "performing simulation using the simulation platform", where what is meant is "performing simulation using the simulation program".

Claim 4 refers to "structuring a simulation platform for use in an architecture design by using the sources; performing the evaluation of the performance of the bus by using the simulation platform", where what is meant is "structuring a simulation program for use in an architecture design by using the sources; performing the evaluation of the performance of the bus by using the simulation program".

Claim 4 refers to "restructuring the simulation platform in response to the modified sources; and performing the evaluation again on the performance of the bus by using the restructured simulation platform", where what is meant is "restructuring the simulation program in response to the modified sources; and performing the evaluation again on the performance of the bus by using the restructured simulation program".

Claim 5 refers to "wherein structuring the simulation platform for use in an architecture design using the sources comprises the steps of", where what is meant is "wherein structuring the simulation program for use in an architecture design using the sources comprises the steps of".

Claim 7 refers to "structuring a simulation platform for use in an architecture design by compiling the sources being modified; performing calculation on the bus traffic for the bus by executing the simulation platform", where what is meant is "structuring a simulation program for use in an architecture design by compiling the sources being modified; performing calculation on the bus traffic for the bus by executing the simulation program".

Claims objected to but not specifically addressed are objected to, based on their dependency to an objected claim.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

9.1 Claim 1, Lines 8-9 state, "in response to modified sources, structuring a simulation platform for use in an architecture design". Specification Page 6, Lines 22-25 state, "a simulation platform is structured to perform architecture design by using sources ...in simulation platform structuring process, the flow proceeds to step A3 to effect isolation of hardware and software". Therefore it is understood that structuring the simulation platform involves isolation of the hardware and software.

Specification page 2, Lines 1-7 state, "Prior to actual manufacturing, simulation platforms (or algorithms) are normally structured without consideration of distinctions between hardware and software... Next, isolation of hardware and software is performed on the structured

simulation platforms, which are divided into hardware elements and software elements respectively. The isolation of hardware and software is made by experiments".

As explained in Paragraph 3 above, what is meant by the simulation platform is the simulation program. It does not involve any hardware. Therefore the structuring of simulation platform involving ***isolation of hardware and software*** mentioned in Specification, Page 6, Lines 22- 25 is not understood. One of ordinary skill in the art will understand that bus operations involve both bus hardware and bus operational software. There is much interaction between hardware and software. Any simulation model of the bus operation will involve both the hardware models and the software models. Therefore it is not understood as to why one will isolate hardware and software in any simulation model of bus operations and how it will affect the simulated bus performance. It is also not understood as to how "The isolation of hardware and software is made by experiments". The specification does not state as to what criteria and process are used to isolate the hardware and software during structuring the simulation platform. Therefore the process of structuring the simulation platform is not properly described in the specification.

9.2 Claim 4 refers to, "structuring a simulation platform for use in an architecture design by using the sources". The process of structuring the simulation platform is not properly described in the specification, as explained in Paragraph 7.1 above.

Claim 4 refers to, "restructuring the simulation platform in response to the modified sources". The process of restructuring the simulation platform is not properly described in the specification, as explained in Paragraph 7.1 above.

9.3 Claim 5 refers to, "wherein structuring the simulation platform for use in an architecture design using the sources comprises the steps of". The process of structuring the simulation platform is not properly described in the specification, as explained in Paragraph 7.1 above.

9.4 Claim 7 refers to "structuring a simulation platform for use in an architecture design by compiling the sources being modified". The process of structuring the simulation platform is not properly described in the specification, as explained in Paragraph 7.1 above.

9.5 Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

10. Claims 6 and 8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10.1 Claim 6 states, "the evaluation is performed on the performance of the bus by using the evaluation function, so that in response to the bus traffic that is finally produced with respect to the processing rate of the bus, isolation of the hardware and software is optimized". The specification does not describe anywhere how this isolation of the hardware and software is

optimized. It does not describe the objective function and the process used for optimization of the isolation of the hardware and software.

10.2 Claim 8 states, "the variables loaded onto the bus consist of n bits while the bus consists of m bits (where n, m are both integral numbers, and n ≤m), so that the bus traffic for the processing rate is produced such that a number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate". It is not understood as to why "a number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate" and how it affects the bus traffic or the processing rate evaluations and the design of the bus architecture. The specification does not state why "a number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate" and how it affects the bus traffic or the processing rate evaluations and the design of the bus architecture.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 1, 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al.** (U.S. Patent 6,269,467) in view of **Tseng et al.** (U.S. Patent 6,321,366), and further in view of **Swoboda et al.** (U.S. Patent 6,546,505).

13.1 **Chang et al.** teaches block based design methodology. Specifically, as per claim 1, **Chang et al.** teaches a bus performance evaluation method for algorithm description in which evaluation is performed on performance of a bus (CL27, L14-27; CL27, L29-31; CL27, L51-54; CL29, L29-34); and

in response to modified sources, structuring a simulation platform for use in an architecture design (CL52, L6-8; CL52, L20-28; Cl52, L29-37; CL52, L47-50).

Chang et al. does not expressly teach a bus interconnecting between hardware and software. **Tseng et al.** teaches a bus interconnecting between hardware and software (CL36, L11-20; CL39, L39-41), because that allows selective control of data delivery across the software/hardware boundary (CL39, L39-41). It would have been obvious to one of ordinary

skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Tseng et al.** that included a bus interconnecting between hardware and software. The artisan would have been motivated because that would allow selective control of data delivery across the software/hardware boundary.

Chang et al. does not expressly teach that evaluation is performed on performance of a bus by using sources described by a general purpose high-level language for verification of an algorithm. **Swoboda et al.** teaches that evaluation is performed on performance of a bus by using sources described by a general purpose high-level language for verification of an algorithm (CL45, L20-28; CL45, L43-52; CL5, L42-44; CL5, L56-60), because the delivery of data to the algorithms in simulation is readily performed by programming to Read and Write to register (CL45, L20-21 and L31-32); and the high level language code is tailored according to the needs of a given application (CL5, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Swoboda et al.** that included evaluation being performed on performance of a bus by using sources described by a general purpose high-level language for verification of an algorithm. The artisan would have been motivated because the delivery of data to the algorithms in simulation would be readily performed by programming to Read and Write to register; and the high level language code would be tailored according to the needs of a given application.

Chang et al. does not expressly teach modifying the sources when data transfer is caused on the bus. **Swoboda et al.** teaches modifying the sources when data transfer is caused on the

bus (CL45, L31-38), because the delivery of data to the algorithms in simulation is readily performed by programming to Read and Write to register (CL45, L20-21 and L31-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Swoboda et al.** that included modifying the sources when data transfer was caused on the bus. The artisan would have been motivated because the delivery of data to the algorithms in simulation would be readily performed by programming to Read and Write to register.

Chang et al. does not expressly teach modifying the sources by executing a specific evaluation function. **Tseng et al.** teaches modifying the sources by executing a specific evaluation function (CL14, L63 to CL15, L1; CL4, L28-3; CL61, L16-23), because evaluation data transfer among logic devices occurs across the interconnects and the buses (CL102, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Tseng et al.** that included modifying the sources by executing a specific evaluation function. The artisan would have been motivated because evaluation data transfer among logic devices would occur across the interconnects and the buses.

13.2 As per claim 4, **Chang et al.** teaches a bus performance evaluation method for algorithm description in which evaluation is performed on performance of a bus (CL27, L14-27; CL27, L29-31; CL27, L51-54; CL29, L29-34);

structuring a simulation platform for use in an architecture design (CL52, L6-8; CL52, L20-28; Cl52, L29-37; CL52, L47-50);

performing the evaluation of the performance of the bus (CL27, L14-27; CL27, L29-31; CL27, L51-54; CL29, L29-34), by using the simulation platform (CL29, L29-34; CL33, L53-59; CL40, L16-19);

restructuring the simulation platform in response to the modified sources (CL52, L6-8; CL52, L20-28; Cl52, L29-37; CL52, L47-50);

performing the evaluation again on the performance of the bus (CL27, L14-27; CL27, L29-31; CL27, L51-54; CL29, L29-34), by using the restructured simulation platform (CL29, L29-34; CL33, L53-59; CL40, L16-19).

Chang et al. does not expressly teach a bus interconnecting between hardware and software. **Tseng et al.** teaches a bus interconnecting between hardware and software (CL36, L11-20; CL39, L39-41), because that allows selective control of data delivery across the software/hardware boundary (CL39, L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Tseng et al.** that included a bus interconnecting between hardware and software. The artisan would have been motivated because that would allow selective control of data delivery across the software/hardware boundary.

Chang et al. does not expressly teach that evaluation is performed on performance of a bus by using sources described by a general purpose high-level language for verification of an algorithm. **Swoboda et al.** teaches that evaluation is performed on performance of a bus by

using sources described by a general purpose high-level language for verification of an algorithm (CL45, L20-28; CL45, L43-52; CL5, L42-44; CL5, L56-60), because the delivery of data to the algorithms in simulation is readily performed by programming to Read and Write to register (CL45, L20-21 and L31-32); and the high level language code is tailored according to the needs of a given application (CL5, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Swoboda et al.** that included evaluation being performed on performance of a bus by using sources described by a general purpose high-level language for verification of an algorithm. The artisan would have been motivated because the delivery of data to the algorithms in simulation would be readily performed by programming to Read and Write to register; and the high level language code would be tailored according to the needs of a given application.

Chang et al. does not expressly teach modifying the sources in response to result of the evaluation of the performance of the bus. **Swoboda et al.** teaches modifying the sources in response to result of the evaluation of the performance of the bus (CL45, L31-38), because the delivery of data to the algorithms in simulation is readily performed by programming to Read and Write to register (CL45, L20-21 and L31-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Swoboda et al.** that included modifying the sources in response to result of the evaluation of the performance of the bus. The artisan would have been motivated because the delivery of data to the algorithms in simulation would be readily performed by programming to Read and Write to register.

13.3 As per claim 9, **Chang et al., Tseng et al.** and **Swoboda et al.** teach the bus performance evaluation method of Claims 1 and 4. **Chang et al.** does not expressly teach that the general purpose high-level language is C language or C++ language. **Swoboda et al.** teaches that the general purpose high-level language is C language or C++ language (CL5, L42-44; CL5, L56-60), because the high level language code is tailored according to the needs of a given application (CL5, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Swoboda et al.** that included the general purpose high-level language being C language or C++ language. The artisan would have been motivated because the high level language code would be tailored according to the needs of a given application.

14. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al.** (U.S. Patent 6,269,467) in view of **Tseng et al.** (U.S. Patent 6,321,366), and further in view of **Swoboda et al.** (U.S. Patent 6,546,505) and **Dangelo et al.** (U.S. Patent 5,801,958).

14.1 As per claim 2, **Chang et al., Tseng et al.** and **Swoboda et al.** teach the bus performance evaluation method of Claim 1. **Chang et al.** teaches performing simulation using the simulation platform to allow calculation of bus traffic for a processing rate of the bus (CL29, L29-34; CL33, L53-59; CL40, L16-19);

so that the evaluation of the performance of the bus is performed (CL27, L14-27; CL27, L29-31; CL27, L51-54; CL29, L29-34).

Chang et al. does not expressly teach that the evaluation of the performance of the bus is performed at a high-level stage of design. **Dangelo et al.** teaches that the evaluation of the performance of the bus is performed at a high-level stage of design (CL69, L59-65), because such preliminary estimate of bus performance can be used in making high level design decisions relating to the system performance, allowing the designer to make intelligent design decisions (CL68, L28-30; L32-34). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Dangelo et al.** that included the evaluation of the performance of the bus being performed at a high-level stage of design. The artisan would have been motivated because such preliminary estimate of bus performance could be used in making high level design decisions relating to the system performance, allowing the designer to make intelligent design decisions.

14.2 As per claim 3, **Chang et al., Tseng et al., Swoboda et al.** and **Dangelo et al.** teach the bus performance evaluation method of Claim 1. **Chang et al.** teaches comprising the step of feeding back result of the evaluation of the performance of the bus to the sources used in the verification of the algorithm (CL52, L6-8; CL52, L20-28; Cl52, L29-37; CL52, L47-50).

Chang et al. does not expressly teach that the architecture design is performed at a high-level stage of design. **Dangelo et al.** teaches that the architecture design is performed at a high-level stage of design (CL69, L59-65), because such preliminary estimate of bus performance can be used in making high level design decisions relating to the system performance, allowing the designer to make intelligent design decisions (CL68, L28-30; L32-34). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Dangelo et al.** that included the architecture design being performed at a high-level stage of design. The artisan would have been motivated because such preliminary estimate of bus performance could be used in making high level design decisions relating to the system performance, allowing the designer to make intelligent design decisions.

15. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al.** (U.S. Patent 6,269,467) in view of **Tseng et al.** (U.S. Patent 6,321,366), and further in view of **Swoboda et al.** (U.S. Patent 6,546,505) and **Fujiwara et al.** (U.S. Patent 6,510,541).

15.1 As per claim 5, **Chang et al., Tseng et al.** and **Swoboda et al.** teach the bus performance evaluation method of Claim 4. **Chang et al.** teaches structuring the simulation platform for use in an architecture design using the sources (CL52, L6-8; CL52, L20-28; Cl52, L29-37; CL52, L47-50).

Chang et al. does not expressly teach analyzing the sources by prescribed units respectively to isolate a hardware portion and a software portion. **Fujiwara et al.** teaches analyzing the sources by prescribed units respectively to isolate a hardware portion and a software portion (Fig. 2, Item 302; CL8, L13-14; CL8, L42-44; CL9, L60-61), because each specification is described with a language capable of representing state transfer logic (CL8, L21-23); data stored in hardware section is described with a hardware description language such as Verilog or VHDL and data stored in software section is described in C/C++ source code (CL10, L9-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Fujiwara et al.** that included analyzing the sources by prescribed units respectively to isolate a hardware portion and a software portion. The artisan would have been motivated because each specification would be described with a language capable of representing state transfer logic; data stored in hardware section would be described with a hardware description language such as Verilog or VHDL and data stored in software section would be described in C/C++ source code.

Chang et al. does not expressly teach creating an evaluation function for counting bus traffic of the bus; and effecting syntax correction on the sources by executing the evaluation function every time data transfer is caused on the bus. **Tseng et al.** teaches creating an evaluation function for counting bus traffic of the bus; and effecting syntax correction on the sources by executing the evaluation function every time data transfer is caused on the bus (CL14, L63 to CL15, L1; CL4, L28-3; CL61, L16-23), because evaluation data transfer among logic devices occurs across the interconnects and the buses (CL102, L1-3). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Tseng et al.** that included creating an evaluation function for counting bus traffic of the bus; and effecting syntax correction on the sources by executing the evaluation function every time data transfer is caused on the bus. The artisan would have been motivated because evaluation data transfer among logic devices would occur across the interconnects and the buses.

15.2 As per claim 6, **Chang et al., Tseng et al.** and **Swoboda et al.** teach the bus performance evaluation method of Claim 4. **Chang et al.** teaches a bus performance evaluation method for algorithm description wherein evaluation is performed on performance of a bus (CL27, L14-27; CL27, L29-31; CL27, L51-54; CL29, L29-34)

Chang et al. does not expressly teach that the evaluation is performed on the performance of the bus by using the evaluation function. **Tseng et al.** teaches that the evaluation is performed on the performance of the bus by using the evaluation function (CL14, L63 to CL15, L1; CL4, L28-3; CL61, L16-23), because evaluation data transfer among logic devices occurs across the interconnects and the buses (CL102, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Tseng et al.** that included the evaluation being performed on the performance of the bus by using the evaluation function. The artisan would have been motivated because evaluation data transfer among logic devices would occur across the interconnects and the buses.

Chang et al. does not expressly teach that in response to the bus traffic that is finally produced with respect to the processing rate of the bus, isolation of the hardware and software is optimized. **Fujiwara et al.** teaches that in response to the bus traffic that is finally produced with respect to the processing rate of the bus, isolation of the hardware and software is optimized (Fig. 2, Item 302; CL8, L13-14; CL8, L42-44; CL9, L60-61), because each specification is described with a language capable of representing state transfer logic (CL8, L21-23); data stored in hardware section is described with a hardware description language such as Verilog or VHDL and data stored in software section is described in C/C++ source code (CL10, L9-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Fujiwara et al.** that included in response to the bus traffic that was finally produced with respect to the processing rate of the bus, isolation of the hardware and software being optimized. The artisan would have been motivated because each specification would be described with a language capable of representing state transfer logic; data stored in hardware section would be described with a hardware description language such as Verilog or VHDL and data stored in software section would be described in C/C++ source code.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
August 20, 2004